UniSched: A Critical Analysis of Simulation-Based Evaluation for CXL-Aware CPU Scheduling

Anonymous Author(s)
Anonymous Institution
anonymous@example.com

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Abstract

Compute Express Link (CXL) is reshaping datacenter memory hierarchies, introducing new latency and bandwidth tiers that challenge traditional CPU scheduling assumptions. We propose UniSched, a proactive, PMU-driven cross-NUMA scheduling framework designed for deployability via Linux's sched$_ext$ mechanism. Unlike prior kernel-modification-based approaches, UniSched aims to provide topology-aware scheduling without requiring kernel patches. We validate PMU profiling overhead on real hardware (0.
event simulations comparing UniSched against Linux EEVDF, AutoNUMA, and Tiresias-like reactive schedulers. However, our simulation reveals a critical finding: all schedulers exhibit statistically identical performance (p=0.999), achieving approximately 8.42 tasks/sec
—specifically, the failure to adequately stress-test CXL topology under concurrent memory bandwidth sat
based evaluation of memory-aware scheduling policies.

1 Introduction

Modern datacenter servers are experiencing a fundamental architectural shift driven by heterogeneous memory hierarchies enabled by Compute Express Link (CXL). A typical server now features multiple memory tiers: local DDR5 DRAM (80–100 ns latency, high bandwidth), CXL-attached DRAM (150–300 ns latency, asymmetric bandwidth), and CXL memory pools shared across sockets (200–500 ns latency) li2023pond, almaruf2023tpp.

Linux 6.12 introduced sched$_ext$, a revolutionary framework enabling custom CPU schedulers as eBP
modification-free scheduling policies that can respond to CXL topology without requiring deep kernel int
aware scheduling but require kernel modifications for page-table self-replication (PTSR) and rely on re
fault-based migration.

The Critical Gap. Current schedulers treat CPU scheduling decisions in isolation from memory topology. When selecting a CPU for a task, schedulers consider CPU load and cache topology but largely ignore where the task's memory resides, leading to suboptimal placement decisions on CXL-enabled systems.

Our Approach. We propose UniSched, a scheduling framework with three key components: (1) topology discovery and characterization, (2) proactive per-task memory profiling via hardware PMUs, and (3) a unified scoring function that balances compute efficiency with memory access efficiency.

Key Findings and Lessons Learned. Despite a comprehensive experimental design, our simulation-based evaluation reveals that all schedulers--including our proposed UniSched--achieve statistically identical performance ($p = 0.999$). This unexpected result led us to discover fundamental limitations in how our simulator models memory contention and CXL topology stress. Rather than presenting marginal "improvements" that fall within statistical noise (0.008% for UniSched Full vs. EEVDF, $p = 0.999$), we use this paper to:

1. Document the discrepancy between expected and observed results
2. Analyze *why* the simulator fails to differentiate scheduling policies
3. Propose specific modifications needed for meaningful evaluation
4. Discuss the broader implications for simulation-based systems research

2 Related Work

2.1 CXL Memory Systems

CXL enables memory expansion and pooling beyond traditional DIMM slots li2023pond. Pond li2023pond demonstrated CXL-based memory pooling for cloud platforms, while TPP almaruf2023tpp introduced transparent page placement for tiered memory systems. NOMAD xiang2024nomad proposed transactional page migration for non-exclusive memory tiering. These works focus on memory management rather than CPU scheduling coordination.

2.2 NUMA-Aware Scheduling

AutoNUMA arcangeli2012autonuma, the production Linux mechanism, uses reactive page sampling and migration. However, it predates CXL and lacks explicit modeling of CXL latency/bandwidth characteristics. Lepers et al. lepers2015thread demonstrated the importance of asymmetry awareness in NUMA scheduling.

2.3 CXL-Aware CPU Scheduling

Tiresias tang2024tiresias is the most closely related work, demonstrating CXL-aware process scheduling through kernel modifications and PTSR. However, Tiresias requires kernel patches and uses reactive page-fault-driven migration.

CXLAimPod yang2025cxlaimpod also uses sched$_e xt for CXL-aware schedulingbutaddressesa f u$
$intra-noderead/writeduplexoptimizationratherthancross-NUMAplacement.UniSchedandCXLAi$
$--UniScheddecideswhichNUMAnode, whileCXLAimPodoptimizeswithinthatnode.$

2.4 User-Space Scheduling

ghOSt humphries2021ghost demonstrated fast user-space delegation of Linux scheduling, paving the way for frameworks like sched$_e xtvernet2024schedext.Shena$
$sensitiveworkloadsthroughcarefulscheduling.$

3 Method

3.1 System Architecture

UniSched consists of three components:

Component 1: Topology Discovery. Enumerate memory tiers via /sys/devices/system/node/ interfaces. Characterize each NUMA node as local DRAM, CXL-attached, or CPU-less. Build latency/bandwidth matrices using PMU-based microbenchmarks.

Component 2: Proactive Per-Task Memory Profiling. Leverage Intel PEBS or AMD IBS to sample memory accesses at $\sim$1% frequency. Track per-task statistics: access distribution across NUMA nodes, bandwidth consumption. Classify tasks as "local-dominant," "cxl-bandwidth-bound," or "latency-sensitive."

Component 3: Unified Scheduling Algorithm. The scheduler scores

CPU candidates using:

$$\begin{aligned} \texttt{score}(\texttt{CPU}, \texttt{task}) = \; & w_1 \cdot \texttt{compute\_score}(\texttt{load}, \texttt{priority}) \\ & + w_2 \cdot \texttt{memory\_score}(\texttt{pattern}, \texttt{NUMA}) \\ & + w_3 \cdot \texttt{migration\_cost}(\texttt{cache\_warmth}) \end{aligned} \tag{1}$$

where $w_1 = 0.4$, $w_2 = 0.4$, $w_3 = 0.2$.

3.2 Implementation Approach

Due to kernel version constraints (available: 6.8.0, required: 6.12+), we adopt a discrete-event simulation approach calibrated with real hardware PMU measurements.

4 Experiments

4.1 Hardware Validation: PMU Overhead

Before simulation, we validate PMU profiling overhead on real hardware using the STREAM benchmark:

- Hardware: Intel Xeon E7-4850 v4 (64 cores, 4 NUMA nodes)
- Baseline bandwidth: 3.55 GB/s
- PEBS sampling at 1%: 0.35% overhead
- PEBS sampling at 2%: 0.89% overhead

The PMU overhead validation passes our 3% gate criterion, confirming the viability of PMU-based profiling.

4.2 Simulation Setup

Topology Configuration. Our simulator models a 4-node NUMA system:

- Node 0-1: Local DRAM (80ns latency, 200 GB/s)
- Node 2: CXL-attached (200ns latency, 80 GB/s)
- Node 3: CXL-remote (350ns latency, 60 GB/s)

Workloads. Five workload types with varying memory access patterns:

1. graph_pagerank: Iterative graph analytics with high memory footprint
2. latency_sensitive: Pointer-chasing with low cache hit rate
3. mixed_workload: Combination of compute and memory-bound tasks
4. redis_ycsb: Key-value store with Zipfian distribution
5. stream_bandwidth: Sequential memory access, bandwidth-bound

Baselines. We compare against:

- EEVDF: Linux default scheduler (simulated)
- AutoNUMA: EEVDF with reactive page migration
- Tiresias-like: Reactive page-fault-driven migration
- CXLAimPod: Intra-node duplex optimization

UniSched Variants. We evaluate ablated versions:

- UniSched_TopologyOnly: No per-task profiling
- UniSched_ProfilingOnly: No topology-aware scoring
- UniSched_NoCoord: No memory coordination
- UniSched_Full: Complete system

4.3 Main Results

Table 1 presents the primary performance comparison. All schedulers achieve approximately 8.42 tasks/sec with no statistically significant differences.

Statistical Significance. Paired t-tests reveal no significant differences between any scheduler pairs:

4.4 Why All Schedulers Show Identical Performance

Our analysis identifies four key simulator limitations that prevent meaningful differentiation:

1. Inadequate Memory Latency Impact Modeling. The simulator's latency penalty factor:

$$\texttt{latency\_factor} = 1.0 + (\texttt{weighted\_latency} - 80)/500.0 \qquad (2)$$

Table 1: Main performance comparison across all schedulers. Values shown as mean ± std across 135 experiments per scheduler. Best results in **bold**. ↑ means higher is better. Note: Differences are not statistically significant ($p > 0.99$).

Method	Throughput (tasks/s) ↑	Avg Latency (ms) ↓	Fairness ↑
EEVDF	8.42 ± 3.84	1329.6	0.748
AutoNUMA	8.42 ± 3.84	1329.5	0.748
Tiresias	8.42 ± 3.84	1329.6	0.748
CXLAimPod	8.41 ± 3.83	1334.8	0.754
UniSched_Full	8.42 ± 3.84	1329.0	0.748
UniSched_TopologyOnly	**8.43** ± 3.84	**1324.8**	0.750
UniSched_ProfilingOnly	8.42 ± 3.84	1329.6	0.748
UniSched_NoCoord	8.42 ± 3.84	1329.0	0.748

Table 2: Statistical significance tests for UniSched Full vs. baselines.

Comparison	Improvement	p-value	Cohen's d	Significant
UniSched vs EEVDF	0.008%	0.999	0.001	No
UniSched vs AutoNUMA	0.008%	0.999	0.001	No
UniSched vs Tiresias	0.008%	0.999	0.001	No
UniSched vs CXLAimPod	0.22%	0.661	0.022	No

produces only a 54% maximum slowdown for CXL-remote memory (350ns). For tasks with durations of 50-500ms, this latency difference is negligible compared to total execution time.

2. Lack of Memory Bandwidth Contention. The simulator models memory latency but does not adequately model memory bandwidth saturation. CXL links have significantly lower bandwidth than local DRAM (60-80 GB/s vs. 200 GB/s), but our workloads do not generate sufficient concurrent memory traffic to saturate these links.

3. Abundant CPU Resources. With 64 CPUs and workloads of 50-100 tasks, CPU resources are not contested. All schedulers can find available CPUs without queueing delays, masking the benefits of intelligent placement.

4. Simplified Migration Costs. Cache warmth and TLB effects are modeled heuristically with fixed costs, not capturing the true performance impact of migrations in real systems.

Table 3: Ablation study results. All differences are statistically insignificant ($p > 0.99$).

Configuration	Throughput (tasks/s)	Migrations
EEVDF	8.42	0
UniSched TopologyOnly	8.43	0
UniSched ProfilingOnly	8.42	0
UniSched NoCoord	8.42	0
UniSched Full	8.42	0

Table 4: Success criteria evaluation.

Criterion	Target	Achieved	Status
PMU Overhead	$\leq 3\%$	0.35%	**PASS**
Throughput Improvement	$\geq 5\%$	0.008%	**FAIL**
Fairness	≥ 0.85	0.748	**FAIL**
Deployability	0 kernel lines	0 (BPF)	**PASS**

4.5 Ablation Study Results

Table 3 presents results for UniSched ablations. Like the main results, differences are within statistical noise.

4.6 Success Criteria Evaluation

Table 4 evaluates our original success criteria.

5 Discussion: Lessons Learned and Simulator Limitations

5.1 What Went Wrong?

Our simulation fails to show meaningful performance differences because it inadequately models the scenarios where CXL-aware scheduling would matter:

1. Insufficient Memory Pressure: Workloads do not saturate CXL bandwidth, making bandwidth-aware placement irrelevant.

2. Task Duration vs. Latency Mismatch: Long-running tasks (50-500ms) amortize memory latency costs that would be significant for short, latency-sensitive operations.

3. CPU Over-provisioning: With more CPUs than concurrent tasks, scheduling decisions have minimal impact on completion times.

5.2 Required Simulator Modifications

To demonstrate meaningful scheduler differences, the simulator requires:

1. Bandwidth Contention Modeling. Implement proper memory bandwidth accounting:

- Track per-link bandwidth utilization
- Model queueing delays when bandwidth is saturated
- Include CXL controller contention for shared resources

2. Workload Characterization. Design workloads that stress CXL topology:

- High-memory-bandwidth tasks that saturate CXL links
- Latency-sensitive microservices with sub-millisecond response requirements
- Memory-intensive co-located workloads competing for CXL bandwidth

3. CPU Contention. Reduce CPU over-provisioning:

- Increase workload concurrency relative to CPU count
- Model CPU time-sharing overhead accurately

4. Realistic Migration Costs. Improve migration modeling:

- Cache warmth decay based on actual access patterns
- TLB shootdown costs for page migrations
- NUMA-remote cache line invalidation overheads

5.3 Broader Implications for Systems Research

Our experience highlights a critical challenge in systems research: simulation validity. A simulator that passes sanity checks (correct latencies, proper topology) may still fail to capture the dynamics that make scheduling decisions meaningful.

Recommendation: Simulation-based scheduler evaluations should include:

1. Sensitivity analysis showing where differences emerge
2. Validation that the simulator can reproduce known behaviors
3. Explicit discussion of limitations and their impact on conclusions

6 Conclusion

We proposed UniSched, a deployable CXL-aware CPU scheduling framework using proactive PMU-based profiling. While we validated the PMU overhead on real hardware (0.35%, well within our 3% target), our simulation-based evaluation revealed that all schedulers achieve statistically identical performance ($p = 0.999$).

Rather than reporting marginal "improvements" that are indistinguishable from noise (0.008% for UniSched Full, $p = 0.999$), we have presented a detailed analysis of why our simulation fails to differentiate scheduling policies. The key issues are inadequate modeling of memory bandwidth contention, insufficient CPU resource pressure, and workloads that do not stress CXL topology.

Our work serves as a cautionary tale for simulation-based systems research and provides concrete recommendations for simulator improvements. Future work should focus on (1) implementing the simulator modifications we identified, (2) validating on real CXL hardware when available, and (3) developing workload suites specifically designed to stress heterogeneous memory hierarchies.

Broader Impact

This work contributes to the understanding of CXL-aware scheduling and highlights the importance of rigorous simulation validation. By openly discussing negative results and simulator limitations, we hope to improve the quality of systems research methodology.

References

[Arcangeli(2012)] Andrea Arcangeli. AutoNUMA: Automatic NUMA balancing. *Linux Kernel Documentation*, 2012-2024.

[Fried et al.(2019)] Joshua Fried, Qizhe Cai, Maxim Planck, and Amy Ousterhout. Shenango: Achieving high CPU efficiency for latency-sensitive datacenter workloads. In *16th USENIX Symposium on Networked Systems Design and Implementation (NSDI 19)*, pages 361-378, 2019.

[Humphries et al.(2021)] Jack Tigar Humphries, Neel Natu, Ashwin Chaugule, Ofir Weisse, Barret Rhoden, Josh Don, Luigi Rizzo, Oleg Rombakh, Paul Turner, and Christos Kozyrakis. ghOSt: Fast & flexible user-space delegation of Linux scheduling. In *Proceedings of the 28th ACM Symposium on Operating Systems Principles*, pages 588-603, 2021.

[Al Maruf et al.(2023)] Hasan Al Maruf, Hao Wang, Abhishek Dhanotia, Johannes Weiner, Niket Agarwal, Pallab Bhattacharya, Chris Petersen, Mosharaf Chowdhury, Shobhit Kanaujia, and Prakash Chauhan. TPP: Transparent page placement for CXL-enabled tiered-memory. In *Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 3*, pages 742-755, 2023.

[Li et al.(2023)] Huaicheng Li, Daniel S Berger, Lisa Hsu, Daniel Ernst, Pantea Zardoshti, Monish Shah, Samir Rajadnya, Scott Lee, Ishwar Agarwal, Mark D Hill, et al. Pond: CXL-based memory pooling systems for cloud platforms. In *Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2*, pages 574-587, 2023.

[Lepers et al.(2015)] Baptiste Lepers, Vivien Quéma, and Alexandra Fedorova. Thread and memory placement on NUMA systems: Asymmetry matters. In *USENIX Annual Technical Conference*, pages 277-289, 2015.

[Raybuck et al.(2021)] Amanda Raybuck, Tim Stamler, Wei Zhang, Mattan Erez, and Simon Peter. HeMem: Scalable tiered memory management for big data applications and real NVM. In *Proceedings of the ACM SIGOPS 28th Symposium on Operating Systems Principles*, pages 392-407, 2021.

[Tang et al.(2024)] Wenda Tang, Tianxiang Ai, and Jie Wu. Tiresias: Optimizing NUMA performance with CXL memory and locality-aware process scheduling. In *Proceedings of the ACM Turing Award Celebration Conference-China 2024*, pages 1-6, 2024.

[Vernet et al.(2024)] David Vernet, Tejun Heo, Andrea Righi, et al. The current status and future potential of sched_ext. In *Linux Plumbers Conference*, 2024.

[Vuppalapati & Agarwal(2024)] Midhul Vuppalapati and Rachit Agarwal. Tiered memory management: Access latency is the key! In *Proceedings of the ACM SIGOPS 30th Symposium on Operating Systems Principles*, pages 79-94, 2024.

[Xiang et al.(2024)] Lingfeng Xiang, Zhenlin Lin, Weishu Deng, Hui Lu, Jia Rao, Yifan Yuan, and Ren Wang. NOMAD: Non-exclusive memory tiering via transactional page migration. In *Proceedings of the 18th USENIX Symposium on Operating Systems Design and Implementation (OSDI 2024)*, 2024.

[Yang et al.(2025)] Yiwei Yang, Yusheng Zheng, Yiqi Chen, Zheng Liang, Kexin Chu, Zhe Zhou, Andi Quinn, and Wei Zhang. CXLAimPod: CXL memory is all you need in AI era. *arXiv preprint arXiv:2508.15980*, 2025.

A Detailed Workload Characteristics

Table 5: Detailed workload characteristics used in simulation.

Workload	Access Pattern	Local DRAM	CXL Memory	Footprint
graph_pagerank	Iterative/High footprint	50%	50%	1–8 GB
latency_sensitive	Random/Pointer-chasing	90%	10%	100 MB
mixed_workload	Balanced	60%	40%	100 MB–2 GB
redis_ycsb	Zipfian/Read-heavy	75%	25%	100 MB
stream_bandwidth	Sequential/Bandwidth	50%	50%	100 MB–2 GB

B Simulator Parameters

Table 6: Key simulator parameters and their sources.

Parameter	Value	Source
Local DRAM latency	80 ns	CXL 2.0 spec
CXL-attached latency	200 ns	CXL 2.0 spec
CXL-remote latency	350 ns	CXL 2.0 spec
Local DRAM bandwidth	200 GB/s	Measured
CXL bandwidth	60–80 GB/s	CXL 2.0 spec
PMU sampling overhead	0.35%	Measured
Scheduling latency	5 μs	Estimated
Migration cost	100 μs	Literature

C Full Statistical Results

`Note: All differences between schedulers are statistically insignificant` ($p > 0.6$).

Table 7: Performance by workload type (throughput in tasks/s).

Scheduler	Graph	Latency	Mixed	Redis	STREAM
EEVDF	8.88	14.34	6.45	8.98	3.47
AutoNUMA	8.88	14.34	6.45	8.98	3.47
Tiresias	8.88	14.34	6.45	8.98	3.47
CXLAimPod	8.88	14.27	6.43	8.98	3.47
UniSched Full	8.88	14.34	6.45	8.98	3.47
UniSched Topology	**8.92**	14.34	**6.46**	**8.98**	**3.48**
UniSched Profile	8.88	14.34	6.45	8.98	3.47
UniSched NoCoord	8.88	14.34	6.45	8.98	3.47